ABSTRACT

A system is disclosed in which an on-chip logic analyzer (OCLA) includes one or more word recognizers. The word recognizer includes a great deal of flexibility for the user, while being capable of implementation with very few gates. The word recognizer includes a Boolean logic portion in which a plurality of conditions can be dynamically segregated into a mutually-exclusive set of groups. The conditions in each group are combined by means of a single Boolean function that is programmable. The resultant term (or product) from each group is combined with those of the other groups by a fixed selection of Boolean functions. The output of the Boolean logic section is provided to a counter/timer. The counter/timer may be configured to either count the number of cycles that the match condition existed, or the number of times a match condition occurred. The counter can also be programmed to count total cycles when the match condition existed, or only consecutive cycles. The counter can be initially programmed with an initial value, and if that value counts out, can be reloaded with a second count value, thereby providing increased flexibility in detecting and selecting state data for storage in an on-chip memory.